Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **N. G2A**
5. **N. G2A**
6. **G1**
7. **Y7**
8. **GND**
9. **Y6**
10. **Y5**
11. **Y4**
12. **Y3**
13. **Y2**
14. **Y1**
15. **Y0**
16. **VCC**

**.065”**

**.065”**

**10**

**9**

**8**

**7**

**15 14 13 12 11**

**2 3 4 5 6**

**16**

**1**

**MASK**

**REF**

**LS138F**

**GS**

**1**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0038” X .0038”**

**Backside Potential: GND or FLOAT**

**Mask Ref: LS138F**

**APPROVED BY: DK DIE SIZE .065” X .065” DATE: 3/29/18**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54LS138**

**DG 10.1.2**

#### Rev B, 7/19/02